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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
TAKASHI KARIYA, ET AL.	: EXAMINER: NEIL ABRAMS
SERIAL NO: 10/564,200	:
FILED: JANUARY 11, 2006	: GROUP ART UNIT: 2839
FOR: INTERPOSER AND MULTILAYER PRINTED WIRING BOARD	:

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal from a non-final Office Action mailed January 25, 2010. A Notice of Appeal was timely filed on June 26, 2010.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is IBIDEN CO., LTD., 1, Kandacho 2-chome, Ogaki-shi, Gifu, Japan 503-8604.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative and the assignees are aware of no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-3 and 5-22 are pending, stand rejected and are herein appealed. Claim 4 is canceled.

IV. STATUS OF THE AMENDMENTS

No amendments have been made after final action in this case. The attached Appendix VIII reflects Claims 1-3 and 5-22 as presently pending on appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 recites an interposer configured to be located between a package substrate made of resin and an IC chip.[1] The interposer includes an insulating base material.[2] A Young's modulus of the insulation base material is 55 to 400 GPa, and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate.[3] A plurality of through holes are provided through the insulating base material.[4] Each of the plurality of through holes has a diameter of 125 μm or less and has formed therein a through hole conductor for connecting the package substrate with the IC chip.[5] The plurality of through holes in the insulating base material are arranged in the form of a grid.[6] Similarly, independent Claim 11 recited an interposer configured to be located between a package substrate made of resin and an IC chip.[7] The interposer includes an insulating base material.[8] A Young's modulus of the insulation base mater is 55 to 440 GPa and a thickness

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[1] See Fig. 3 and page 14, lines 18-22 of the specification.
[2] See Fig. 2 and page 14, lines 22-27 of the specification.
[3] See page 4, lines 12-22 of the specification.
[4] See Fig. 3 and page 14, lines 22-25 of the specification.
[5] See Fig. 3 and page 8, line 31 - page 9, line 5 of the specification.
[6] See page 9, lines 5-7 of the specification.
[7] See Fig. 3 and page 14, lines 18-22 of the specification.
[8] See Fig. 2 and page 14, lines 22-27 of the specification.

of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate.[9] A plurality of through holes are provided through the insulating base material.[10] Each of said plurality of through holes has a diameter of 125 μm or less and has formed therein a through hole conductor for connecting said package substrate with the IC chip.[11] The plurality of through holes in the insulating base material are arranged in the form of a staggard arrangement.[12]

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3 and 5-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,204,563 to Ouchi et al., U.S. Patent 6,828,666 to Herrell et al., U.S. Patent 6,452,807 to Berrett, U.S. Patent 4,667,219 to Lee et al., U.S. Patent 4,825,284 to Soga et al., U.S. Patent 6,670,699 to Mikubo et al. and U.S. 6,516,513 to Milkovich et al. This ground of rejection is presented for review in this appeal.

VII. ARGUMENTS

A. The Cited References Do Not Disclose the Claimed Thickness of the Insulating Base recited in Claims 1 and 11.

As noted above and shown in the claims appendix, independent Claims 1 and 11 recite that "a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate." With regard to this feature, the Office Action states

> Ouchi, figure 1, includes an interposer 3 to be located between a substrate 9 and an IC chip 1, the interposer ... is ***depicted to have a thickness that appears to clearly be within the recited ratio of 0.05 to 1.5 times the thickness of the substrate...***[13]
>
> As to ***insulation base thickness limitations while Ohuchi is seen as entirely sufficient,*** interposer bases within the recited ratio range are ***also***

[9] See page 4, lines 12-22 of the specification.
[10] See Fig. 3 and page 14, lines 22-25 of the specification.
[11] See Fig. 3 and page 8, line 31 - page 9, line 5 of the specification.
[12] See page 9, lines 5-7 of the specification.
[13] Office Action at paragraph linking pages 2 and 3 (emphasis added).

> ***shown*** in Harrell, figure 1 at 113, Soga at 9, Barrett at 10 and Mikubo at 3. Also obvious, should the matter be at issue, to use such relationships for Ohuchi interposer base since that ***appears to be a standard way to form such interposer to minimize size of the assembly.***

Thus, the Action concludes that the claimed thickness relationship feature is disclosed in the prior art based solely on the manner in which the interposer and substrate are depicted in the drawings of the cited references. However, none of the cited references disclose scaled drawings by which one could measure and calculate the thickness range based solely on the drawings. In this regard, it is well settled that proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale.[14]

The Office Action attempts to remedy this deficiency by concluding that the claimed thickness feature "appears to be a standard way to form such interposer to minimize size of the assembly," as also seen in the above quote. However, the Action does not provide any additional evidence or reasoning in support of this conclusion. Thus, the Office Action's conclusion of the "standard way" to form an interposer is, again, based on the drawings alone, which as noted above, cannot support a teaching of a standard because they are not to scale. Moreover, none of the above cited references discuss anything about thickness values of the interposer in relation to the package substrate. Surely, one skilled in the art would not look to a depiction in the drawings for a particular thickness ratio which is nowhere mentioned in any of the cited references. That is, one of ordinary skill in the art reading the cited references would not conclude that any standard thickness ratio taught by the cited references.

For the above reasons, Appellants respectfully submit that the Office Action has not presented a *prima facie* case that the feature of "a thickness of the insulating base material is

[14] MPEP §2125.

0.05 to 1.5 times the thickness of the package substrate" is taught or suggested by the cited references.

B. Claims 1 and 11 are Not Obvious Over the Cited references.

Even assuming that the claimed thickness feature (and all other claim features) are taught by the cited references as the Office Action asserts, Appellants submit that one of ordinary skill in the art would not find it obvious to combine the teaching of the cited references to arrive at the claimed invention. As noted above, the claimed invention includes a ***combination*** of design features for the interposer, which was discovered by the inventors to suppress deformation of the insulation base material and reduce the occurrence of a crevice or breaking in a resin layer of an IC connected to the interposer.[15] Specifically, as noted above and seen in the claims Appendix, each of Claims 1 and 11 include the following combination of features:

(1) a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate

(2) Young's modulus of the insulation base material is 55 to 440 GPa

(3) each of the plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip

(4) wherein the plurality of through holes in the insulating base material are arranged in the form of a grid (Claim 1) or staggered arrangement (Claim 11).

As discussed in the Background section of Appellants' specification, it is generally known to provide an interposer between an IC chip and a package substrate in order to relieve

[15] See specification at page 7, line 14 - page 8, line 3.

stress caused by different thermal expansion properties of the IC chip and substrate. [16] As also noted in the Background, however, the inventors recognized that high frequency IC chips having a low-K resin wiring layer are brittle and, thus, particularly prone to cracking under thermal stress. That is, the inventors recognized that thermal stress defects can occur in an IC chip having the low-k wiring layer, despite the use of an interposer.[17] Appellants' invention is directed to improving the capability of the interposer to absorb thermal stress in order to reduce the possibility of defects in the brittle low-k wiring layer of an IC chip.

In particular, the present inventors conducted extensive experiments to identify a combination of interposer design parameters for reducing thermal stress to a low-K resin layer of an IC chip associated with the interposer. The results of these experiments are shown in Figures 12-16 and corresponding portions of Appellants' specification.

Regarding the combination of features (1) and (2) noted above, Figure 15 of Appellants' demonstrates that a thickness ratio from 0.05 to 1.5 provides a relatively low stress applied to the brittle wiring layer of the IC. This range was determined with due consideration of the change in Young's modulus caused by through holes in the interposer, as shown in Figs. 16A-16B. Further, the upper layer of the thickness range is significant because one of ordinary skill in the art may conclude that a greater thickness in the interposer would provide increased rigidity and isolation from the thermal expansion of the package substrate. As seen in Fig. 15, an increase in thickness may actually result in greater stress to the wiring layer of the IC, contrary to what would be expected by one skilled in the art.

Thus, even if separate teachings of the claimed Young's modulus and the claimed thickness range can be found in the prior art, one of ordinary skill in the art would not combine these teachings without having the benefit of Applicants' disclosure.

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[16] See specification at paragraph linking pages 1 and 2.
[17] See specification at paragraph linking pages 1 and 2.

With regard to the claimed through hole diameter in feature (3), as discussed in Appellants' specification, when the diameter of the through hole is 125 μm or less, the amount of heat generation increases in the through holes because conductor resistance increases. The claimed invention is directed to this particular situation in which a small diameter through hole (125 μm or less) generates excessive heat. The Office Action admits that Ouichi et al. does not teach the hole size feature, but states,

> "... As to hole size ***it would have been obvious to select the smallest holes size necessary to achieve the desired current.*** ... So applied, Ohuchi is fully adequate for claims 1 and 11."

However, the Office Action fails to identify a "desired current" in Ohuchi et al. which would lead to the claimed hole size. Thus, even assuming that a desired current correlates to a hole size, there is no way for one of ordinary skill in the art to arrive at the claimed hole size from Ohuchi et al.. Thus, the Office Action fails to establish that Ohuchi et al. teaches the claimed hole size feature.

In an effort to remedy this deficiency, the Office Action states,

> In addition, for the hole size feature, note Milkovich column 6, lines 65-65, reference to "4 mils" for size of pads at ends of holes, the holes then likely having diameters in range of about 2 to 3 mil. Such dimensions, even if holes size 4 mils, is within the recited claims 1, 11 range. ***Obvious to use such 4 mils or less size for Ohuchi holes to provide a small size component.***[18]

However, the cited reference to Milkovich et al. relates to a multilayer interposer wherein material composition of the various layers transition from properties close to the IC chip to properties close to the package substrate. There is no discussion in Milkovich et al. or Ohuchi et al. of providing a small size component, and the Office Action does not explain how a small size component is consistent with Ohuchi et al. Appellants respectfully submit

[18] Office Action at page 3, lines 9-16.

that the above statement does not provide adequate reasoning to support a conclusion of obviousness.

Finally, feature (4), the inventors determined that the effect of heat generated by small sized through holes can be mitigated by a particular arrangement of the through holes. As noted above, when the diameter of the through hole is small, the amount of heat generation increases in the through holes because conductor resistance increases. Where the through holes are disposed in the form of the grid (as in Claim 1) or in the staggered fashion (as in Claim 11), "the temperature distribution of the interposer at the time of usage becomes uniform so that no stress concentrates on any specific location thereby the insulation layer of the IC chip being not damaged. Further, the physical property (thermal expansion coefficient, Young's modulus and the like) of the insulation base material just below the IC chip becomes uniform because the through holes are formed uniformly."[19]

Nevertheless, the Action states,

> Obvious to use such grid feature in Ohuchi and for claim 11 to use a staggered grid. With these arrangements a larger numbers of circuit paths is possible.

However, the Action does not explain how a larger number of "circuit paths" is possible, or even why it is desirable to have a large number of circuit paths in the configuration of Ohuchi et al, or any other cited reference. Thus, the Office Action's reasoning cannot support the conclusion of obviousness.

As noted above, Appellants specification explains that high frequency ICs use a "low-K" resin wiring layer which is brittle and prone to cracking under thermal stress. Thus, stress defects in the IC chip occur during loading of the substrate with the IC.[20] As discussed above, the inventors discovered that the combined features of the claimed incention provide

[19] Appellants' specification at paragraph 23.
[20] See specification at paragraph linking pages 1 and 2.

an improved configuration that suppresses deformation of the insulation base material and reduces the occurrence of a crevice or breaking in the resin layer of the IC. None of the six references combined for rejecting Claims 1 and 11 disclose any reason for combining the recited features, and the Office Action does not provide sufficient reasoning to support the conclusion of obviousness. Thus, Appellants submit that combination of these claimed features is impermissible hindsight reasoning based on Appellants' disclosure.

Thus, the cited references do not disclose or render obvious the combination noted above.

C. None of the cited references disclose the feature of Claims 8 and 17.

Dependent Claims 8 and 17 recite that the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole. As discussed in Appellants' specification, this feature provides advantages of reducing heat and thermal stress in the area of the through hole.[21] The Office Action does not explicitly address this feature, and thus, the Action does not provide a prima facie rejection of Claims 8 and 17. Further, none of the cited references disclose the features of Claims 8 and 17.

D. None of the cited references disclose the features of Claims 20 and 25

Further, Claims 20 and 21 specify that the a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid to effect substantially uniform temperature of the interposer. Similarly, Claim 22 recites that the plurality of through holes are arranged at substantially equal distance from each other. As discussed in Appellant's specification, these features further reduce thermal stress on the interposer.[22] The Office Action does not explicitly

[21] Appellants' specification at paragraph 24.
[22] Appellants' specification at paragraph 23.

address this feature, and thus, the Action does not provide a *prima facie* rejection of Claims 20-22. Further, none of the cited references disclose the features of Claims 20-22.

CONCLUSION

For the reasons discussed above, all pending claims patentably define over the cited references. Therefore, the rejection should be reversed.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

Claim 1: An interposer configured to be located between a package substrate made of resin and an IC chip, the interposer comprising:

an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440 GPa and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate; and

a plurality of through holes provided through the insulating base material, ~~at~~ each of said plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip,

wherein the plurality of through holes in the insulating base material are arranged in the form of a grid.

Claim 2: The interposer according to Claim 1, wherein the thickness of said insulation base material is at least 0.08 times the thickness of core of the package substrate.

Claim 3: The interposer according to Claim 1, wherein the size of said insulation base material is equal to or larger than a projection area of an electronic component loaded on the interposer, and equal to or less than a projection area of the package substrate.

Claim 5: The interposer according to Claim 1, wherein said package substrate is a multilayer printed wiring board.

Claim 6: The interposer according to Claim 1, wherein said through hole conductor is made of metal plating.

Claim 7: The interposer according to Claim 1, wherein said through hole conductor is made of metallic paste.

Claim 8: The interposer according to Claim 1, wherein as regards the sectional shape of the through hole in the insulation base material, the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole.

Claim 9: A multilayer printed wiring board having the interposer according to Claim 1.

Claim 10: The interposer according to Claim 1, wherein a diameter of each of the plurality of through holes is from 30 μm to 125 μm.

Claim 11: An interposer configured to be located between a package substrate made of resin and an IC chip, the interposer comprising:

an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440 GPa and a thickness of said insulation base material is 0.05 to 1.5 times the thickness of the package substrate; and

a plurality of through holes provided through the insulating base material,

each of said plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting said package substrate with the IC chip,

wherein the plurality of through holes in the insulating base material are arranged in the form of a staggard arrangement.

Claim 12: The interposer according to Claim 11, wherein a thickness of said insulation base material is at least 0.08 times the thickness of core of the package substrate.

Claim 13: The interposer according to Claim 11, wherein the size of said insulation base material is equal to or larger than projection area of an electronic component loaded on the interposer, and equal to or less than a projection area of the package substrate.

Claim 14: The interposer according to Claim 11, wherein said package substrate is a multilayer printed wiring board.

Claim 15: The interposer according to Claim 11, wherein said through hole conductor is made of metal plating.

Claim 16: The interposer according to Claim 11, wherein said through hole conductor is made of metallic paste.

Claim 17: The interposer according to Claim 11, wherein as regards the sectional shape of the through hole in the insulation base material, the diameter of an opening in at

least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the through hole.

Claim 18: A multilayer printed wiring board having the interposer according to Claim 11.

Claim 19: The interposer according to Claim 11, wherein a diameter of each of the plurality of through holes is from 30 μm to 125 μm.

Claim 20: The interposer according to Claim 1, wherein a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid.

Claim 21: The interposer according to Claim 20, wherein the plurality of through holes are arranged to effect substantially uniform temperature of the interposer.

Claim 22: The interposer according to Claim 1, wherein each of the plurality of through holes are arranged at substantially equal distance from each other.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.